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21CS33

Third Semester B.E. Degree Examination, Jan./Feb. 2023
Analog and Digital Electronics

Time: 3 hrs.

Max. Marks: 100

Note: *Answer any FIVE full questions, choosing ONE full question from each module.*

Module-1

1   a. Derive an expression for collector current and collector emitter voltage of voltage divider bias circuit (accurate analysis). **(08 Marks)**
     b. Explain relaxation oscillator. **(06 Marks)**
     c. Sketch and explain the working of Peak detector. **(06 Marks)**

OR

2   a. Explain R-2R ladder type DAC with a neat diagram. **(06 Marks)**
     b. List the advantages of active filters over passive filters. **(06 Marks)**
     c. For the circuit shown in Fig. Q2 (c) below find the value of R_1 and R_2 if supply voltages are +12 and −12 V. Assume hysteresis with −6 V.
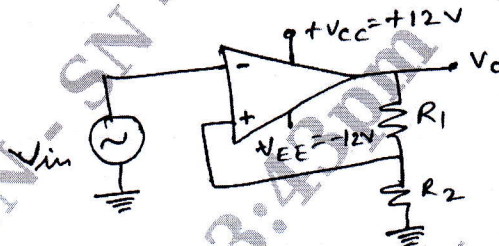

Fig. Q2 (c)

(08 Marks)

Module-2

3   a. Find all the prime implicates of the function,
         $f(a, b, c, d) = \Pi(0,2,3,4,5,12,13) + \Pi d(8,10)$
         using the Quine-McCluskey method. **(10 Marks)**
     b. Plot the Karnaugh maps and find all the minimal sums and minimal products of the following Boolean functions.
         (i) $f(a, b, c) = \sum(2,4,5,6,7)$
         (i) $f(a, b, c) = \Pi(1,4,5,6)$ **(10 Marks)**

OR

4   a. With an example, explain Petrik's method. **(06 Marks)**
     b. For the given Boolean function, determine a minimal sum and a minimal product using MEV techniques using a, b and c as the map variables.
         $f = \sum(3,4,5,7,8,11,12,13,15)$ **(08 Marks)**
     c. Explain Entered variable map method. **(06 Marks)**

Important Note : 1. On completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages.
2. Any revealing of identification, appeal to evaluator and /or equations written eg, 42+8 = 50, will be treated as malpractice.

Module-3

5   a. Explain the importance of three-state buffer.   (06 Marks)
    b. With a neat diagram, explain 3 to 8 line decoder.   (06 Marks)
    c. What is a multiplexer? Write the logic diagram for 8 : 1 multiplexer using 4 input AND and OR gates.   (08 Marks)

OR

6   a. Discuss different types of hazards in combinational circuits.   (08 Marks)
    b. Distinguish between combinational and sequential circuit.   (06 Marks)
    c. Write a note on PLA and PAL.   (06 Marks)

Module-4

7   a. Explain the working of JK master slave flip-flop with a sketch, truth table and symbol.   (06 Marks)
    b. What is D flip flop? Illustrate the operation of the clear and preset inputs in D-flip-flop with timing diagram.   (08 Marks)
    c. What is VHDL? Show how to model the 4 to 1 multiplexer using a VHDL conditional assignment statement.   (06 Marks)

OR

8   a. What is T-flip-flop? Show how to convert D-flip flop into T-flip-flop.   (08 Marks)
    b. What are the three different models for writing a module body in VHDL? Give example for any one model.   (06 Marks)
    c. Explain with a neat diagram, VHDL program structure.   (06 Marks)

Module-5

9   a. With a neat diagram, explain 4-bit parallel adder with accumulator.   (10 Marks)
    b. Define counter. Design mod-5 counter using J-K flip flop.   (10 Marks)

OR

10 a. With neat diagram, explain 4 bit SISO register.   (08 Marks)
    b. Mention the Application of shift registers.   (05 Marks)
    c. Explain the working of a 3 bit shift register.   (07 Marks)

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